UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,863	07/02/2003	Jason A. Goldstein	7257/115(a)	4392

23381 7590 06/29/2006

DORR, CARSON & BIRNEY, P.C.
ONE CHERRY CENTER
501 SOUTH CHERRY STREET
SUITE 800
DENVER, CO 80246

EXAMINER	
KIM, HAROLD J	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,863	GOLDSTEIN, JASON A.	
	Examiner	Art Unit	
	Harold Kim	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/25/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
Supervisory PRIMARY EXAMINER 6/16/2006
GROUP 2100 AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030825, 20030702*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 9-32 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 30-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms are lack of proper antecedent basis:

i. said connection mapping interconnects - claim 30, line 5;

ii. said connection mapping - claim 31, line 1;

iii. said interconnects - claim 31, lines 1-2;

iv. said second memory device - claim 32, line 1.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 9-32 are rejected under 35 U.S.C. 102(e) as being anticipated by

Swenson et al., US Patent no. ~~6,684,275~~ 5,926,120.

6. In re claim 9, Swenson et al. shows a method for performing serial data to parallel data conversion [fig 5A],

serially receiving a data word at a serial data input interface [SERIAL IN, fig 5A];

providing said received data word to a serial-to-parallel mapping circuit [71-74 in fig 5A];

partitioning said provided received data word into a plurality of partitioned received data words [71-74 in fig 5A];

generating memory write control signals and memory write address signals [C3, ADDRESS 79 in fig 5A];

directing said generated memory write control signals and said generated memory write address signals to a memory device [C3, 79, RAM in fig 5A];

writing said partitioned provided received data words to said memory device in response to said directing [79, RAM in fig 5A];

generating memory read control signals and memory read address signals [79, BIT SELECT 85 in fig 5A];

directing said memory read control signals and said memory read address signals to said memory device [79, BIT SELECT 85, RAM in fig 5A];

reading an output data word from said memory device in response to said directing said direct said memory read control signals and said memory read address signals [79, 85 in fig 5A and 5B]; and

reordering bits of said output data word to provide a parallel output data word [101-104 in fig 5B].

7. In re claim 10, Swenson et al. shows said partitioning is performed by said serial-to-parallel mapping circuit [fig 5A].

8. In re claim 11, Swenson et al. shows said generating said memory write control signals and said memory write address signals is performed by said serial-to-parallel mapping circuit [C3, ADDRESS 79 in fig 5A].

9. In re claim 12, Swenson et al. shows said directing said generated memory write control signals and said generated memory write address signals comprises directing said signals to a first port of said memory device [RAM, fig 5A].

10. In re claim 13, Swenson et al. shows writing said partitioned provided received data words to uniquely associated memory addresses in said memory device [RAM, A(0)0, B(0)0 in fig 5A].

11. In re claim 14, Swenson et al. shows directing said signals to a second port of said memory device [82, M2 in fig 5A].

12. In re claim 15, Swenson et al. shows reading said output data word with an output mapping circuit [RAM, 101-104 in figs 5A, and 5B].

13. In re claim 16, Swenson et al. shows mapping interconnects between an output port of an output mapping circuit and an input port of a parallel output interface [M2, 84, 101-104, and PARALLEL OUT in fig 5B].

14. In re claim 17, Swenson et al. shows providing a clock rate for said serial-to-

parallel mapping circuit which is at least

15. eight times faster than a clock rate for said serial data input interface [col 6, lines 37-62].

16. In re claim 18, Swenson et al. shows a method for conducting parallel data to serial data conversion [fig 5A], the method comprising:

receiving a parallel data word [PARALLEL IN, fig 5A];

reordering at least one bit of said received parallel data word to provide a reordered parallel data word [75-78, fig 5A];

writing said reordered parallel data word to a memory device [RAM, fig 5A];

reading output data from said memory device [81, M1, fig 5A];

partitioning said read output data into a plurality of serial data words [91-94, fig 5B]; and

providing a serially converted output data word from said plurality of partitioned serial data words [95-95, SERIAL STREAM OUT, fig 5B].

17. In re claim 19, Swenson et al. shows receiving said parallel data word at a parallel-to-serial input mapping circuit [75-78, fig 5A].

18. In re claim 20, Swenson et al. shows reordering said received parallel data word at a parallel-to-serial input mapping circuit [75-78, fig 5A].

19. In re claim 21, Swenson et al. shows writing said reordered received parallel data word to a first port of said memory device [tx(0)0, RAM in fig 5A].

20. In re claim 22, Swenson et al. shows reading data from a second port of said

memory device [M1, 81 in fig 5A].

21. In re claim 23, Swenson et al. shows mapping interconnects between a parallel-to-serial input mapping circuit and said memory device [M1, 83, 91-94, fig 5B].

22. Claims 24-27 are rejected same rationale as claims 9-23.

23. In re claim 28, Swenson et al. shows a serial-to-parallel and parallel-to-serial converter [figs 5A and 5B] comprising:

a serial data input interface [SERIAL IN, fig 5A] for receiving a serial input data word;

an input memory [RAM, fig 5A] connected to said serial data input interface and responsive to said receiving to converted said serial input data word into a parallel output data word [RX0-RX3 in fig 5B], said input memory including a first memory device [RAM, fig 5A] having a two memory banks [tx(0)3 to tx(0)0, and D(0)0 to A(0)0 in fig 5A], which two memory banks allow writing of data to a first of said two memory banks simultaneous with reading of data from a second of said two memory banks [RAM in fig 5A];

serial communication lines [SERIAL IN, fig 5A] coupled to said input memory and operative to output said parallel output data word onto a parallel data bus [PARALLEL OUT in fig 5B];

an output memory [91-94 in fig 5B] operative to receive a parallel input data word [PARALLEL IN, fig 5A] from said parallel data bus and to convert said received parallel input data word into a plurality of serial data words [SERIAL STREAMS OUT, fig 5B], said output memory including a second memory device [95-98 in fig 5B]; and

a serial data output interface [95-98 in fig 5B] for receiving said plurality of serial data words and for providing a serially converted output data word.

24. In re claim 29, Swenson et al. shows a serial-to-parallel mapping circuit [71-74 in fig 5A] responsive to said receiving to provide write control signals [C3] and write address signals [Address 79] to said first memory device.

25. In re claim 30, Swenson et al. shows an output mapping circuit [91-94, 101-104 in fig 5B] in communication with said first memory device;

a parallel output interface [PARALLEL OUT, fig 5B]; and

a connection between said output mapping circuit and said parallel output interface, said connection mapping interconnects between an output port of said output mapping circuit and an input port of said parallel output interface [fig 5B].

26. In re claim 31, Swenson et al. shows said connection mapping said interconnects is operative to reorder at least one bit of an output data word from said first memory device to provide said parallel output data word [101-104, fig 5B].

27. In re claim 32, Swenson et al. shows said second memory device includes two second-memory-device memory banks [tx(0)3 to tx(0)0, and D(0)0 to A(0)0 in fig 5A], which two memory banks allow writing of data to a first of said two second-memory-device memory banks simultaneous with reading of data from a second of said two second-memory-device memory banks [RAM, fig 5A].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Further references of interest are cited on Form PLO-892, which is attachment to this office action.

Any response to this action should be mailed to:

Mail Stop ____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The centralized fax number is 571-273-8300.

The centralized hand carry paper drop off location is:

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop _____
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application should be directed to the central telephone number (571) 272-2100.

Direct any inquiries concerning drawing review to the Drawing Review Branch (703) 305-8404.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harold Kim whose telephone number is 571-272-4148. The examiner can normally be reached on Monday-Friday 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Harold J. Kim
Patent Examiner
June 22, 2006/HK

Supervisory

fritz m. fleming
FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
Au 181
6/26/2006